UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/090,489	03/04/2002	Ranjit S. Oberoi	5681-14000	5065

7590 02/23/2005

Jeffrey C. Hood
Conley, Rose, & Tayon, P.C.
P.O. Box 398
Austin, TX 78767

EXAMINER	
LEE, HWA C	
ART UNIT	**PAPER NUMBER**
2672	

DATE MAILED: 02/23/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/090,489	OBEROI ET AL.+	
	Examiner	Art Unit	
	Hwa C Lee	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *7-10,13,14 and 17-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *7-10, 13-14, and 17-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/04/2004 has been entered.

Response to Arguments

2. Applicant's arguments filed 10/04/2004 have been fully considered but they are not persuasive. The applicant continues to assert the same argument that Brunner teaches pixel by pixel accumulation, while the applicant recites accumulating all pixels from an image with a second image at the same time. This however is without merit since a careful read of the claims 7 and 17 does not explicitly pixel accumulation different from Brunner. The applicant correctly states that Brunner teaches using several accumulators, which explicitly is accumulating a plurality of pixels together before displaying said pixels.

3. Applicant's arguments with respect to claims 7-10, 13-14, and 17-24 have been considered but are moot in view of the new ground(s) of rejection. The examiner agrees that Brunner does not teach accumulating a sequence of images (video). However, upon further consideration, a new ground(s) of rejection is made in view of Morein as

applied below. Said new grounds of rejection are necessitated by the amendment filed 10/04/2004.

Claim Cancellations

4. Claims 1-6, 11-12, and 15-16 are cancelled by the applicant.

Claim Objections

5. Claim 21 is objected to because of the following informalities: Claim 21 is currently dependent on claim 21. For art rejection purpose, claim 21 will be treated as being dependent on claim 18. Appropriate correction is required.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

8. Claims 7, 9-10 and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morein, US Patent No.: 6,457,034 in view of Haeberli et al., Journal Publication (Computer Graphics, Volume 24, Number 4, August 1990).

9. In regards to claim 7, Morein and Haeberli et al. in combination clearly teach a method comprising: ***(a) reading a first stream of image pixels corresponding to an image X_K from an image buffer; (b) reading a second stream of pixels corresponding to an image A_K from an accumulation buffer; (c) blending each image pixel of the image X_K with the corresponding pixel of the image A_K based on an alpha value provided with the image pixel, and thus, generating a third stream of output pixels defining an image A_{K+1}; and (d) transferring the third stream of output pixels to the accumulation buffer; (e) performing (a), (b), (c) and (d) for each image in a sequence of images X_K, K=0, 1, 2, ... , N-1, wherein N is the number of images in the sequence.***

- Morein teaches a method and apparatus for supporting accumulation buffering in a video graphics system (Col. 2, lines 3-36), which explicitly is accumulating each image in a sequence of images X_k, K=0, 1, 2, ... , N-1. All video comprises a sequence of images.
- Morein teaches blending together pixel data from the drawing buffer (140) and the first (170) or second accumulation buffer (180) using the controller (160), which specifically is reading a first stream of image pixels and second stream of image pixels as recited in the instant claim (Col. 5, line 10 – Col. 6, line 12 and FIG. 1). Thus, said drawing buffer specifically is an image buffer. The controller reads the pixel data from the drawing buffer and adds said pixel data to the corresponding pixel data in the accumulation buffer based on the information found in the mask buffer (150). Said mask buffer allows the accumulation

process to be performed efficiently by indicating only the relevant pixel data. In addition, Morein teaches that once a predetermined number of accumulation operations have occurred for a predetermined number of images, said first accumulation buffer acts as the output buffer (Col. 6, lines 13-25). Thus, said blended pixel data is transferred back and stored in the first accumulation buffer. Then the second accumulation buffer takes over the next predetermined set of accumulation processes. In other words, the first and second accumulation buffer takes turn accumulating pixel data for each sequence of image.

- Although Morein does not explicitly teach blending images based on alpha values, it is well known and standard in the art that blending images using accumulation buffer requires alpha blending. Blending a plurality of layers specifically must be performed using not only the color values but also the alpha values. Said alpha values determine the weight given to each image in the set of images being blended together.

10. An analogous art, Haeberli et al. teaches that the accumulation buffer provides 16 bits to store each red, green, blue, and alpha color components (Pages 311, Section 3.2). Thus, by definition, blending the alpha color components of all images being blended specifically is blending based on the alpha value provided with each pixel.

11. It would have been obvious to one of ordinary skill in the art at the time of the invention to take the teachings of Morein and to modify it by adding the method of blending each image pixel based on the alpha value of each image pixel in order to implement standard blending using the accumulation buffer. The alpha values dictate

the opacity of each image pixel, which influence the weighed average of the color values for each pixel, and thus blending by alpha value is a necessary standard technique well known in the art.

12. In reference to claim 9, Morein and Haeberli et al. teach the method of claim 7 as described above. In addition, Morein and Haeberli et al. teach in combination ***said blending comprises blending red, green and blue components of each output pixel in parallel.*** As applied to claim 7 above, all color values are blended together for each pixel (Col. 5, line 26 – Col. 6, line 25). Since Haeberli et al. teaches that accumulation buffers provides storage for RGB and alpha color values, blending color values together as taught by Morein specifically is blending RGB and alpha values together. And since all color values for each pixels are blended together, said blending of RGB and alpha values must be performed in parallel.

13. In reference to claim 10, Morein and Haeberli et al. teach the method of claim 7, but do not explicitly teach wherein (a), (b), (c), (d) and (e) are performed by a graphics hardware accelerator chip in response to software functions executed on a host processor. Although Morein and Haeberli et al. do not explicitly name a ***hardware accelerator***, the prior art discloses the overall architecture of one embodiment where the system is implemented on a processor, a state machine, or other circuitry (Col. 5, lines 26-30 and Col. 7, lines 6-16). Said graphics system comprising an integrated circuit specifically is a hardware accelerator chip performing in response some sort of software commands to perform (a), (b), (c), (d), and (e). Also, the instruction is given via software since that is the conventional method of communication between the

processor and the rest of the graphics hardware. Thus, it would have been obvious to implement the graphics system of Morein and Haeberli et al. using a hardware accelerator chip.

14. In regards to claim 17, the same basis and rationale for claim rejection as applied to claim 7 above. The limitations of claim 17 are identical to the limitations of claim 7, except for one added limitation directed to the mixing unit. Morein explicitly teaches a mixing unit (Col. 5, line 26 – Col. 6, line 25). Said controller (160) specifically is a mixing unit.

15. Claims 8, 18-19, and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morein in view of Haeberli et al., and further in view of McReynolds et al., On-line publication entitled, "Advanced Graphics Programming Techniques Using Open GL."

16. In reference to claims 8 and 18, Morein and Haeberli et al. teach the method of claim 7, but does not explicitly teach ***the color precision of the accumulation buffer is greater than the color precision of the image buffer***. It is well known and obvious, however, to implement a more precise output data calculation in order to avoid losing original data precision and minimize aliasing. An analogous art, McReynolds et al., teaches said limitations.

- McReynolds et al. teaches that 'in order to maintain accuracy over many blending operations, the accumulation buffer has a higher number of bits per color components than a typical color buffer (section 6.4, lines 3-4). Higher

number of bits per color components will result in greater color precision for the accumulation buffer.

17. It would have been obvious to someone of ordinary skill in the art to take the teachings of Morein and Haeberli et al. and to add from McReynolds, the method of providing higher color precision of the accumulation buffer than the color precision of the image buffer in order to maintain color precision accuracy over many blending operations. This prevents loss of data and alleviates aliasing problems. It is always important to maintain precise accuracy of data after any data processing.

18. In reference to claim 19, Morein and Haeberli et al., teach the method and system of claim claims 7 and 17 above, and Morein, Haeberli et al. and McReynolds teach the system of claims 8, 18, and 22 above. In addition, remember that Morein teaches a first and a second accumulator in order to minimize the delay between accumulation and rendering. Since each pixel provides a RGB color component and an alpha value, each of the plurality of accumulators is capable of mixing ***a corresponding color component***. Morein also explicitly teaches that if the color data includes multiple color portions, such as red, green, and blue portions, each of these portions will be treated individually by the output block (Col. 6, lines 37-42), and thus it would have been obvious to one of ordinary skill in the art at the time of the invention to take the teachings of Morein and Haeberli and to implement a plurality of mixing units to accumulate individual color components. Since parallel processing is well known and obvious in the art, it would have been obvious to use a plurality of mixing units to comprise the controller (160) of Morein. This is further suggested by Haeberli et al.

since an accumulator buffer comprises 16 bit to store each red, green, blue, and alpha components, it would be wise to apply a different mixer for each component in order to perform parallel processing and speed up the overall image processing.

19. In reference to claim 22, Morein and Haeberli et al. teach the system of claim 17, and Morein, Haeberli et al. and McReynolds teach the system of claim 18 above. While Morein and Haeberli et al. do not explicitly teach ***the color precision of the accumulation buffer is at least ΔN larger than the color precision of the image buffer, wherein ΔN is the base two logarithm of the maximum number of images to be blended into the accumulation buffer***, McReynolds et al. teaches said limitation in the following in similar fashion as applied to claims 8 and 18 above.

- As applied to claims 8 and 18 above, McReynolds et al. teaches that in order to maintain accuracy over many blending operations, the accumulation buffer has a higher number of bits per color components than a typical color buffer (section 6.4, lines 3-4). Higher number of bits per color components than a typical color buffer is interpreting broadly as to include the bit range ***ΔN larger than the color precision of the image buffer***. The definition of ***ΔN***, base two log of maximum number of images to be blended into the accumulation buffer, is one of design choices resulting in the accumulation buffer having a higher number of bits per color than the image buffer. ΔN as defined by the applicant has no clear advantage over other design choices, and the specific definition still falls under the range of bit size disclosed by McReynolds.

20. It would have been obvious to someone of the ordinary skill in the art to take the teachings of Morein and Haeberli et al. and to take from McReynolds et al. and one of many design choices to modify the bit size of the accumulation buffer to be at least ΔN larger than that of the image buffer, where ΔN is defined as stated in the claim language, in order to maintain color precision accuracy over many blending operations. This is the same motivation as applied to claims 8 and 18 above.

21. Claims 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Morein in view of Haeberli et al., and further in view of McReynolds et al. as applied to claims 8, 18, and 22 above, and further in view of Murata et al., US Patent No.: 5,621,866.

22. In regards to claim 21, Morein, Haeberli et al. and McReynolds et al. teach the system of claim 18 above, but do not explicitly teach ***wherein the image buffer resides within the frame buffer of a graphic system***. It is, however, well known in the art that frame buffer is a memory module storing image information to be sent to the display device (e.g. Monitor), and it is also well known and standard in the art the a memory module can comprise a plurality of separate memory units. This allows for easy transfer of data from one memory to another, especially any image data from image buffer to frame buffer for the purpose of speedy display of said image data. For example, an analogous art, Murata et al. explicity teaches that a frame buffer comprises an image buffer and a Z buffer (Col. 1, lines 33-40; Col. 3, lines 4-37 and FIG. 1(A), 3-4). It would have been obvious to one of ordinary skill in the art at the time of the invention to take the teachings of Morein, Haeberli et al. and McReynolds et al., and to add from Murata et al., the combined image and frame buffer since it is well known and obvious standard

in the art. Having separate buffers in one memory (buffer) module saves space, speeds data transfer and provides overall efficient graphic system.

23. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Morein in view of Haeberli et al., and further in view of McReynolds as applied to claims 8, 18, and 22 above, and further in view of Murata et al. as applied to claim 21 above, and further in view of Takeuchi, US Patent Application No: 2002/0082081.

24. In reference to claim 20, Morein and Haeberli et al., and McReynolds teach the system of claim 18 above, but do not explicitly teach ***the accumulation buffer resides within a texture buffer of a graphics system***. But, remember that Murata et al. explicitly teaches that a plurality of buffers can reside in one large buffer unit. An analogous art, Takeuchi, explicitly teaches one memory module comprising a plurality of buffers including an accumulation buffer (47) and a texture buffer (48) connected as one unit (FIG. 3). Since the accumulation buffer and the texture buffer are indeed connect together in the figure, Takeuchi explicitly teaches an accumulation buffer residing within a texture buffer. In addition, in light of the well know and standard memory allocation technique as taught by Murata, it would have been obvious to one of ordinary skill in the art at the time of the invention to take the teachings of Morein, Haeberli et al., and McReynolds, and to add from Murata et al. and Takeuchi the memory allocation technique to combine a plurality of buffers in one large memory module in order to save space and speed up data transfer as applied to claim 21 above. This effectively eliminate the need for extra individual buffers and to expand the capacities of the texture buffer since a texture buffer can include several SDRAMs capable of housing

several types of buffers and memories. Further, having the accumulation buffer reside in the texture buffer will reduce interconnect lengths and thus improve speed and efficiency of the hardware accelerator.

25. Claims 23 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Morein in view of Haeberli et al. as applied to claims 7 and 17 above, and further in view of Murata et al. as applied to claims 20-21 above, and further in view of Takeuchi as applied to claim 20 above.

26. In regards to claim 23, the same basis and rationale for claim rejection as applied to claims 7, 17, 20, and 21 above. Morein and Haeberli teach the limitations of the claims 7 and 17 above, which are almost identical to the instant claim. Morein and Haeberli however do not explicitly teach that the first pixel image stream is read from the frame buffer. Murata, however, explicitly teaches that the frame buffer comprises an image buffer as applied to clam claim 21 above. In addition, Morein and Haeberli do not explicitly teach that the second stream of pixel image is read from the accumulation buffer allocated in the texture buffer. As applied to claim 20 above, Murata et al. and Takeuchi in combination explicitly teach said limitation. The motivation to combine the references is the same as applied to claims 20 and 21 above.

27. In regards to claim 13, Morein, Haeberli, Murata et al., and Takeuchi teach the graphics system of claim 23 above. In addition, Takeuchi explicitly teaches that the texture buffer is a VRAM, which specifically is a type of a DRAM. Since SDRAM is also a type of a DRAM, it would have been obvious to use either a SDRAM or a VRAM to implement the texture buffer. Further, it is well known in the art that a plurality of RAMs

are available for use in a graphical system and choosing one over the other is a design choice at best. Since the applicant does not explicitly teach the criticality of using SDRAM over any other RAM (e.g. VRAM), Takeuchi reads on the limitation of the instant claim.

28. Claims 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Morein in view of Haeberli et al., and further in view of Tang et al., and further in view of Murata et al. as applied to claim 23 above, and further in view of Baker, Online Publicaiton ("What's New, a Report from SIGGRAPH 98". September 1998).

29. In regards to claim 14, Morein, Haeberli, Murata et al., and Takeuchi et al. do not explicitly teach ***the frame buffer comprises one or more 3D-RAM memory devices***, but it is well known in the art to use any one of a plurality of RAMs for any memory unit. For example, an analogous art, Baker, discloses the said limitation (Page 7, Section 3.3.4: Other Products).

30. It would have been obvious to one of ordinary skill in the art to take the teachings of Morein, Haeberli et al., Murata et al., and Takeuchi et al. and to add from Baker the 3D-RAM frame buffer memory architecture in order to improve 3-D rendering performance. The 3-D RAM frame buffer memory architecture is optimized for high-performance 3D graphics that provides approximately 3-4 fold increase in rendering performance by increasing the data transfer rate by integrating key functions on-chip, including arithmetic logic unit to accelerate Z-buffer rendering and on-chip caches. Thus, the 3-D RAM frame buffer will increase the rendering performance when blending 3-D images.

31. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Morein in view of Haeberli et al., and further in view of Murata et al., and further in view of Takeuchi et al. as applied to claim 23 above, and further in view of Marino, U.S. Patent Publication No. 2003/0137523.

32. In regards to claim 24, Morein and Haeberli do not explicitly teach ***wherein the texture buffer has a configurable pixel depth precision***, but Morein hints at said limitation as applied to claims 8, 18, and 22 above. In addition, an analogous art, Marino, explicitly teach said limitation. Marino teaches that the invention includes a graphics system blending unit that bit slices multipliers, e.g., such as an 8x8 multiplier, so at least two multiplier operations can be performed per cycle per multiplier...plurality of multipliers, and the means for reconfiguring each multiplier of the blending unit to perform at least two operations per cycle (paragraph [0011]-[0015]). Thus, Marino teaches a method to reconfigure 'multipliers' to corresponding bit size of the image pixels to be blended together. In this embodiment, Marino explicitly teaches ***a configurable pixel depth precision***.

33. It would have been obvious to someone of ordinary skill in the art to take the teachings of Morein, Haeberli et al., and Murata et al. and to add from Tang et al. and Marino, the configurable pixel depth precision in order to gain more efficient performance using less memory allocation. Using configurable pixel depth precision eliminates waste by using appropriate size multipliers and memory space to blend image pixels.

Conclusion

34. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. The following teaches that a frame buffer comprises an image buffer.

DeGoricija et al., US Patent No: 5,977,991

Alcorn et al., US Patent No: 6,661,424

Reynolds, US Patent No: 6,747,645

Reynolds, US Patent Application No: 2004/0212624

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hwa C Lee whose telephone number is 703-305-8987. The examiner can normally be reached on M-F 8:00-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi can be reached on 703-305-4713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hwa C Lee
Examiner
Art Unit 2672

HCL
02/16/2005

MICHAEL RAZAVI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600